The Law Offices of Mikio Ishimaru
Intellectual Property Law
Patents - Licensing - Strategy - & Related Matters
333 W. El Camino Real, Suite #330
Sunnyvale, CA 94087
Telephone: (408) 738-0592
Fax: (408) 738-0881

Fax

To:	Mail Stop Amendment Examiner Tu Tu V Ho	From:	Mikio Ishimaru
Fax:	(571) 273-8300 TC 2818	Pages:	31, including this page
Phone:	(571) 272-1778	Date:	November 30, 2005
Re:	U.S. Patent Application Serial No. 10/825,910	Atty Docket no.:	27-017

☒ Response to Office Action and Request to Reinstate Appeal

Certificate of Transmission under 37 CFR 1.8

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on November 30, 2005

Vickie Ishimaru

With reference to serial number 10/825,910, the following are being submitted:

- Fax Cover Sheet with Certificate of Transmission
- Transmittal for Enclosures w/duplicate copy
- Response and Request to Reinstate Appeal

RECEIVED
CENTRAL FAX CENTER

DEC 0 1 2005

Docket No.: 27-017

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Byung Tai Do et al.	**Confirmation No.:**	8877
Serial No.:	10/825,910	**Examiner:**	Tu Tu V Ho
Filed:	Apr 16, 2004	**Group Art Unit:**	2818
For:	THERMALLY ENHANCED STACKED DIE PACKAGE AND FABRICATION METHOD		

TRANSMITTAL FOR ENCLOSURES *(check all that apply)*

- ☒ Response / Amendment
  - ☐ After Final
  - ☐ Affidavits/Declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement, PTO Form-1449, & cited Reference(s)
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Terminal Disclaimer
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Petition to Convert to a Provisional Application
- ☐ Request for Refund
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below):*
  - Fax Cover Sheet with Certificate of Transmission

Remarks

The fee, if required, has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	20	20	0	x $50 =	$ 0.00
Independent Claims	4	4	0	x $200 =	$ 0.00
		If multiple claims newly presented, add $300			
		Fee for extension of time			120.00
		Other:			
				TOTAL FEE	$120.00

☒ Please charge Deposit Account No. 50-0374 in the amount of $120.00. An additional copy of this transmittal sheet is submitted herewith.

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 50-0374, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

12/01/2005 TL0111 00000047 500374 10825910
01 FC:1251 120.00 DA

Mikio Ishimaru
Registration No. 27,449
Date: November 30, 2005

RECEIVED
CENTRAL FAX CENTER

DEC 0 1 2005

Docket No.: 27-017

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Byung Tai Do, et al.	: Confirmation No.:	8877
Serial No.:	10/825,910	: Art Unit:	2818
Filed:	4/16/2004	: Examiner:	Tu Tu V Ho
For:	THERMALLY ENHANCED STACKED DIE PACKAGE AND FABRICATION METHOD	:	

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR REINSTATEMENT OF APPEAL

UNDER 37 CFR § 1.193(B)(2)(ii)

AND

APPEAL BRIEF

Sir:

In response to the Office Action mailed September 30, 2005 in which prosecution was reopened and a restriction requirement issued in response to Applicants' filing of a Pre-Appeal Brief Request for Review, Applicants hereby respectfully request Reinstatement of the Appeal Under 37 CFR § 1.193(b)(2)(ii). The following Appeal Brief is submitted pursuant to the Notice of Appeal filed September 19, 2005 in the above identified Application.

(1) ***Real party in interest:***

The real party in interest is STATS ChipPac Ltd., having its principal place of business at 5 Yishun Street 23, Singapore, 768442, Singapore.

(2) ***Related appeals and interferences:***

There are no known related appeal or interference cases.

(3) ***Status of claims:***

Claims 1-20, the only claims pending, stand under final rejection under 35 U.S.C. §103(a), from which rejection this Appeal is taken.

(4) ***Status of amendments:***

An Amendment after Final Rejection was filed on August 17, 2005 to correct typographical errors in the specification and the drawings. In a telephone conference with the Examiner on 10/12/05, the Examiner indicated that the amendments after final rejection would be entered, but Applicants have not yet received written confirmation of the entry of the amendments to the specification and drawings.

(5) ***Summary of invention:***

1. A method of assembling a semiconductor package [100] with stacked dies comprising:

providing a substrate [102] (p. 4, ln. 30 through p. 5, ln. 4);

attaching a first die [104] to the substrate [102] (p.5, lns. 5-10);

electrically connecting the first die [104] to the substrate [102] (p. 5, lns. 10-15);

attaching a heat sink [200] to the first die [104] (p. 5, lns. 16-29);

the heat sink [200] comprising a body portion [902], an undercut portion [604] around a periphery thereof, and a plurality of legs [904] integrally formed with the undercut portion [604] (p.5, lns. 18-29, p. 9, lns. 6-15);

attaching the plurality of legs [904] to the substrate [102] (p. 9, lns. 9-11);

attaching a second die [300] to the heat sink [200] (p. 5, ln. 30 through p. 6, ln. 3);

electrically connecting the second die [300] to the substrate [102] (p. 6, lns. 4-9); and

encapsulating the first die [104], the heat sink [200], and the second die [300] (p. 6, lns. 12-17).

2. The method of assembling a semiconductor package [100] with stacked dies as claimed in claim 1 wherein:

electrically connecting the first die [104] to the substrate [102] uses a number of bonding wires [108] (p. 5, lns. 10-15); and

attaching a heat sink [200] attaches a heat sink [200] that extends laterally over the number of bonding wires [108] (p. 5, lns. 16-29).

3. The method of assembling a semiconductor package [100] with stacked dies as claimed in claim 1 wherein attaching a heat sink [200] attaches a heat sink [200] that is electrically grounded (p. 7, lns. 23-26).

4. The method of assembling a semiconductor package [500] with stacked dies as claimed in claim 1 wherein attaching a heat sink [600] attaches a heat sink [600] that has an electrically conductive coating [608] (p. 7, lns. 23-26), further comprising:

connecting the second die [700] to the electrically conductive coating [608] (p. 8, lns. 11-22); and

connecting the electrically conductive coating [608] to a ground plane [610] (p. 8, lns. 11-22).

5. The method of assembling a semiconductor package [100] with stacked dies as claimed in claim 1 wherein attaching a heat sink [200] attaches a heat sink [200] that extends laterally beyond the edges of the second die [300] (p. 8, lns. 4-10).

6. A method of thermally enhancing a semiconductor package [100] with a stack of dies comprising providing a heat sink [200] between dies [104] [300] in the stack; the heat sink [200] having a body portion [902], an undercut portion [204] around a periphery thereof, and a plurality of legs [904] integrally formed with the undercut portion [204] (p.5, lns. 18-29, p. 9, lns. 6-15).

7. The method of thermally enhancing a semiconductor package [100] with a stack of dies as claimed in claim 6 wherein:

providing a heat sink [200] attaches a heat sink [200] that extends laterally over the lower die [104] to which the heat sink [200] is attached (p. 5, lns. 16-29).

8. The method of thermally enhancing a semiconductor package [100] with a stack of dies as claimed in claim 6 wherein providing a heat sink [200] attaches a heat sink [200] that is electrically grounded (p. 7, lns. 23-26).

9. The method of thermally enhancing a semiconductor package [500] with a stack of dies as claimed in claim 6 wherein providing a heat sink [600] attaches a heat sink [200] that has an electrically conductive coating [608] (p. 7, lns. 23-26), further comprising:

connecting one of the dies [700] in the stack of dies to the electrically conductive coating [608] (p. 8, lns. 11-22); and

connecting the electrically conductive coating [608] to a ground plane [610] (p. 8, lns. 11-22).

10. The method of thermally enhancing a semiconductor package [100] with a stack of dies as claimed in claim 6 wherein providing a heat sink [200] attaches a heat sink [200] between each adjoining pair of dies [104] [300] in the stack of dies (p. 5, lns. 16-29).

11. A semiconductor package [100] with stacked dies comprising:

a substrate [102] (p. 4, ln. 30 through p. 5, ln. 4);

a first die [104] attached to the substrate [102] (p.5, lns. 5-10);

the first die [104] being electrically connected to the substrate [102] (p. 5, lns. 10-15);

a heat sink [200] attached to the first die [104] (p. 5, lns. 16-29);

the heat sink [200] having a body portion [902], an undercut portion [204] around a periphery thereof, and a plurality of legs [904] integrally formed with the undercut portion [204] (p.5, lns. 18-29, p. 9, lns. 6-15);

the plurality of legs [904] attached to the substrate [102] (p. 9, lns. 9-11);

a second die [300] attached to the heat sink [200] and electrically connected to the substrate [102] (p. 5, ln. 30 through p. 6, ln. 3); and

an encapsulant [800] over the first die [104], the heat sink [200], and the second die [300] (p. 6, lns. 12-17).

12. The semiconductor package [100] with stacked dies as claimed in claim 11 further comprising:

a number of bonding wires [108] electrically connecting the first die [104] to the substrate [102] (p. 5, lns. 10-15); and wherein:

the undercut [204] of the heat sink [200] extends laterally over the number of bonding wires [108] (p. 5, lns. 16-29).

13. The semiconductor package [100] with stacked dies as claimed in claim 11 wherein the heat sink [200] is electrically grounded (p. 7, lns. 23-26).

14. The semiconductor package [100] with stacked dies as claimed in claim 11 wherein:

the heat sink [600] has an electrically conductive coating [608] connected to a ground plane [610] on the substrate [502] (p. 8, lns. 11-22); and

the second die [700] is connected to the electrically conductive coating [608] (p. 8, ln. 11-22).

15. The semiconductor package [100] with stacked dies as claimed in claim 11 wherein the undercut [204] of the heat sink [200] extends laterally beyond the edges of the second die [300] (p. 8, lns. 4-10).

16. A thermally enhanced semiconductor package [100] with a stack of dies comprising:

a heat sink [200] between dies [104] [300] in the stack (p.5, lns. 18-29, p. 9, lns. 6-15);

the heat sink [200] having a body portion [902], an undercut portion [204] around a periphery thereof, and a plurality of legs [904] integrally formed with the undercut portion [204] (p.5, lns. 18-29, p. 9, lns. 6-15).

17. The thermally enhanced semiconductor package [100] with a stack of dies as claimed in claim 16 wherein:

the undercut [204] of the heat sink [200] extends laterally over the die [104] to which the heat sink [200] is attached (p. 5, lns. 16-29).

18. The thermally enhanced semiconductor package [500] with a stack of dies as claimed in claim 16 wherein the heat sink [600] is electrically grounded (p. 7, lns. 23-26).

19. The thermally enhanced semiconductor package [500] with a stack of dies as claimed in claim 16 wherein:

the heat sink [600] has an electrically conductive coating [608] (p. 7, lns. 23-26);

one of the dies [700] in the stack of dies [504] [700] is connected to the electrically conductive coating [608] (p. 8, lns. 11-22) and

the electrically conductive coating [608] is connected to a ground plane [610] (p. 8, ln. 11-22).

20. The thermally enhanced semiconductor package [100] with a stack of dies as claimed in claim 16 wherein a heat sink [200] is positioned between each adjoining pair of dies [104] [300] in the stack of dies (p. 8, lns. 11-22).

(6) Issues Presented

(a) Whether the restriction requirement issued after final rejection in response to Applicants' Pre-Appeal Brief Request for Review was proper.

(b) Whether claims 1, 2, 5-7, 10-12, 15-17, and 20 were properly rejected under 35 U.S.C. §103(a) as being unpatentable over Akram in view of Ho.

(c) Whether claims 3, 8, 13, and 18 were properly rejected under 35 U.S.C. §103(a) as being unpatentable over Akram in view of Ho and further in view of Chiu.

(d) Whether claims 4, 9, 14, and 19 were properly rejected under 35 U.S.C. §103(a) as being unpatentable over Akram in view of Ho further in view of Chiu and further in view of Shin.

(e) Whether claims 1, 2, 5-7, 10-12, 15-17 and 20 were properly rejected under 35 U.S.C. §103(a) as being unpatentable over Ho in view of Akram.

(f) Whether claims 3, 8, 13, and 18 were properly rejected under 35 U.S.C. §103(a) as being unpatentable over Ho in view of Akram and further in view of Chiu.

(g) Whether claims 4, 9, 14, and 19 were properly rejected under 35 U.S.C. §103(a) as being unpatentable over Ho in view of Akram further in view of Chiu and further in view of Shin.

(7) The Restriction Requirement

Applicants filed a Notice of Appeal and Pre-Appeal Brief Request for Review on September 19, 2005 with respect to the Final Rejection of claims 1-20 issued on June 17,

2005. In response to the Pre-Appeal Brief Request for Review, prosecution was reopened and a restriction requirement was issued on September 30, 2005. The Examiner stated that restriction was required between claims 11-20 (Group I) and claims 1-10 (Group II).

Applicants respectfully traverse this restriction requirement because according to 37 C.F.R. §1.142:

> "If two or more independent and distinct inventions are claimed in a single application, the examiner in an Office action will require the applicant in the reply to that action to elect an invention to which the claims will be restricted, this official action being called a requirement for restriction (also known as a requirement for division). Such requirement will normally be made before any action on the merits; however, it may be made at any time before final action." [underlining for clarity]

The Examiner issued the restriction requirement in this case well after the final rejection of the pending claims. Indeed this restriction requirement was issued only after prosecution was reopened in response to the filing of a Notice of Appeal and Pre-Appeal Brief Request for Review.

Additionally, pursuant to the MPEP §808:

> "Every requirement to restrict has two aspects: (A) the reasons (as distinguished from the mere statement of conclusion) why each invention *as claimed* is either independent or distinct from the other(s); and (B) the reasons why there would be a serious burden on the examiner if restriction is not required," [underlining for clarity]

It is axiomatic that the burden on the Examiner referred to herein relates to the burden of conducting a prior art search. In the present case the Examiner had already completed a search of the prior art and formulated the bases of the final rejection of all claims before issuing the restriction requirement. Applicants submit that the second aspect set forth above therefore cannot be met by the Examiner. There was no burden on the Examiner in performing the prior art search.

The restriction requirement issued by the Examiner was improper and should be withdrawn. Such action is hereby solicited.

Nonetheless, in compliance with 37 C.F.R. §1.143, Applicants hereby provisionally elect the claims of Group I.

Serial No.: 10/825,910
Group Art Unit: 2818

(8) Grounds for Rejections:

Rejection #1:

Claims 1, 2, 5-7, 10-12, 15-17, and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Akram (U.S. Patent 6,351,028, hereinafter "Akram"), in view of Ho et al. (U.S. Patent 6,507,104, hereinafter "Ho").

Rejection #2:

Claims 3, 8, 13, and 18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Akram (U.S. Patent 6,351,028, hereinafter "Akram") in view of Ho et al. (U.S. Patent 6,507,104, hereinafter "Ho") as applied above, and further in view of Chiu et al. (U.S. Patent 6,437,984, hereinafter "Chiu").

Rejection #3:

Claims 4, 9, 14, and 19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Akram (U.S. Patent 6,351,028, hereinafter "Akram") in view of Ho et al. (U.S. Patent 6,507,104, hereinafter "Ho"), further in view of Chiu et al. (U.S. Patent 6,437,984, hereinafter "Chiu") as applied above (the '028/104/984 reference), and further in view of Shin et al. (U.S. Patent 5,854,511, hereinafter "Shin").

Rejection #4:

Claims 1, 2, 5-7, 10-12, 15-17 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ho et al. (U.S. Patent 6,507,104, hereinafter "Ho") in view of Akram (U.S. Patent 6,351,028, hereinafter "Akram").

Rejection #5:

Claims 3, 8, 13, and 18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ho et al. (U.S. Patent 6,507,104, hereinafter "Ho") in view of Akram (U.S. Patent 6,351,028, hereinafter "Akram") as applied above (the '104/028 reference), and further in view of Chiu et al. (U.S. Patent 6,437,984, hereinafter "Chiu").

Serial No.: 10/825,910
Group Art Unit: 2818

Rejection #6:

Claims 4, 9, 14, and 19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ho et al. (U.S. Patent 6,507,104, hereinafter "Ho") in view of Akram (U.S. Patent 6,351,028, hereinafter "Akram"), further in view of Chiu et al. (U.S. Patent 6,437,984, hereinafter "Chiu") as applied above (the '104/028/984 reference), and further in view of Shin et al. (U.S. Patent 5,854,511, hereinafter "Shin").

(9) ***Arguments:***

Rejection #1:

Summary of Akram:

Akram is directed to the packaging of more than one integrated circuit device within a common package. Akram discloses the use of a T-interposer between stacked dies in a package. There is no disclosure or suggestion in Akram that the T-interposer does or could have legs connected to a substrate. Therefore, Applicants submit that Akram actually teaches away from Applicants invention as claimed.

Summary of Ho:

Ho is directed to a semiconductor package in which only one semiconductor chip [31] is packaged with a heat sink [33] attached to the semiconductor chip [31] having solder balls [35]. There are no bond wires electrically connecting the semiconductor chip to a substrate.

Arguments:

It is respectfully submitted that claims 1, 2, 5-7, 10-12, 15-17, and 20 are improperly rejected under 35 U.S.C. 103(a), as being unpatentable over Akram in view of Ho.

Applicants' claimed combination, as exemplified in claim 1, includes the limitation not disclosed in Akram or Ho taken either singly or in combination of a semiconductor package having stacked dies in which:

> "the heat sink comprising a body portion, an undercut portion around a periphery thereof, and a plurality of legs integrally formed with the undercut portion"

With regard to claims 1, 6, 11, and 16, with respect to combining Akram and Ho, the Examiner has stated:

> "Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '028 patent' heat sink such that the heat sink has a plurality of legs integrally formed with the undercut portion of the heat sink. One would have been motivated to make such a change so that the plurality of legs provide support for the body portion which is positioned above the semiconductor die, as taught by the '104 patent. A semiconductor package such modified hereinafter is referred to as the '028/104 device, and the combined teachings is referred to as the '028/104 reference."

Applicants respectfully traversed this rejection. Applicants agree with the Examiner that Akram:

> "...fails to teach that the heat sink includes a plurality of legs integrally formed with the undercut portion of the heat sink, and thus further fails to teach attaching the plurality of legs to the substrate."

Ho refers to FIG. 2 in pointing out the drawbacks of the structure of FIG. 2 (see column 2, lines 1-16). Applicants respectfully submit that Ho actually teaches away from the use of a heat sink in a semiconductor package as claimed by Applicants by listing what are perceived to be these drawbacks.

Furthermore, Ho does not disclose or suggest the use of the heat sink shown in FIG. 2 in a semiconductor package having stacked dies. Ho discloses the device in FIG. 2 as prior art. The structure shown in FIG. 2 of Ho shows a heat sink that is exposed through the molding compound of the semiconductor package rendering it impossible to attach an additional semiconductor chip to the heat sink in FIG. 2 because the second semiconductor chip would be outside the semiconductor package rendering the resulting device inoperable. Applicants submit that a combination of references that results in an inoperable device is improper under 35 U.S.C. §103.

In fact, U.S. Patent No. 5,997,626 to Wu, et al (hereinafter Wu), which is referred to by Ho with reference to FIG. 2 at column 1, lines 52-67 states that:

> "Preferably the heat spreader [32] is exposed by the molding compound [30]." (see column 3, lines 53-55 of Wu)

Wu, the patent referred to by Ho, therefore does not disclose or suggest a semiconductor package for stacked dies as claimed by Applicants. Ho does not disclose or suggest that more than one die may be stacked in a single package, and therefore teaches away from Applicants invention.

Since both Akram and Ho teach away from Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103.

Where there is a specific hint or suggestion in a particular reference, but the references as a whole teach away from each other, the combination cannot be obvious according to the CAFC:

> "We have noted elsewhere, as a "useful general rule," that references that teach away cannot serve to create a prima facie case of obviousness... If references taken in combination would produce a "seemingly inoperative device", we have held that such references teach away from the combination and thus cannot serve as predicates for a prima facie case of obviousness." *In re* Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984) [deletion for clarity]

Accordingly, it is submitted that the Examiner's reference to a "028/104 device, and the combined teachings of the '028/104 reference" is improper and without foundation because of *In re* Gordon, *supra* .

Accordingly, Applicants submit that claims 1, 6, 11, and 16 are allowable over Akram and Ho taken either singly or in combination because of *In re* Gordon, *supra.*

With regard to claims 2, 7, 12, and 17, the Examiner has stated:

> "Referring to claims 2, 7, 12, and 17, the '028/104 reference further discloses electrically connecting the first die (24) to the substrate uses a number of bonding wires (no number) and attaching a heat sink attaches a heat sink that extends laterally over the number of bonding wires, that extends laterally over the lower die, and such that the undercut of the heat sink extends laterally over the number of bonding wires."

Applicants traversed this rejection. Referring to claims 2, 7, 12, and 17, these dependent claims respectively depend from independent claims 1, 6, 11, and 16 and are believed to be allowable for the reasons set forth above since they contain all the limitations set forth in the independent claims from which they depend and claim non-obvious combinations thereof.

With regard to claims 5 and 15, the Examiner has stated:

> "Referring to claims 5 and 15, as evident from Figs. 5 and 9 of the '028 reference, the reference further discloses attaching a heat sink attaches a heat sink that extends laterally beyond the edges of the second die."

Applicants respectfully traversed this rejection. Referring to claims 5 and 15, these dependent claims respectively depend from independent claims 1 and 11 and are believed to be allowable for the reasons set forth above since they contain all the limitations set forth in the independent claims from which they depend and claim non-obvious combinations thereof.

With regard to claims 10 and 20, the Examiner has stated:

> "Referring to claims 10 and 20, as evident from Fig. 7, the reference further discloses providing a heat sink attaches a heat sink between each adjoining pair of dies in the stack of dies."

Applicants respectfully traversed this rejection. Referring to claims 10 and 20, these dependent claims respectively depend from independent claims 6 and 16 and are believed to be allowable for the reasons set forth above since they contain all the limitations set forth in the independent claims from which they depend and claim non-obvious combinations thereof.

This rejection should be reversed.

Rejection #2:

Summary of Akram:

Supra

Summary of Ho:

Supra

Summary of Chiu:

Chiu is directed to a semiconductor package that has only one semiconductor chip. Accordingly, Chiu does not disclose or suggest a semiconductor package with stacked dies as claimed by Applicants.

Arguments:

It is respectfully submitted that claims 3, 8, 13, and 18 are improperly rejected under 35 U.S.C. §103(a) as being unpatentable over Akram in view of Ho and further in view of Chiu.

Applicants respectfully traversed this rejection since the Applicants' claimed combination, as exemplified in claim 1, includes the limitation not disclosed in Akram, Ho, or Chiu of a semiconductor package having stacked dies in which:

> "the heat sink comprising a body portion, an undercut portion around a periphery thereof, and a plurality of legs integrally formed with the undercut portion"

With regard to claims 3, 8, 13, and 18, the Examiner has stated:

> "Chiu, in disclosing a thermally enhanced chip scale package having a heat sink (114, Fig. 1B), teaches that the heat sink may be wire bonded to a ground connection to provide the packaged integrated circuit with shielding from electrical or electromagnetic interference (column 2, lines 16-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '028/104 reference's heat sink so that the heat sink is electrically grounded using wire bonding. One would have been motivated to make such a modification in view of the teachings by Chiu that ground connection using wire bonding provide the packaged integrated circuit with shielding from electrical or electromagnetic interference. A semiconductor package such modified hereinafter is referred to as the '028/104/984 device, and the combined teachings is referred to as the '028/104/984 reference."

Applicants respectfully traversed this rejection. As set forth above with respect to claims 1, 6, 11, and 16 it is respectfully submitted that the Examiner's proposed combination of Akram and Ho is improper because of *In re* Gordon, *supra* since each reference teaches away from Applicants' invention, and if combined result in an inoperable device.

Since each of Akram, Ho, and Chiu teach away from Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103. Accordingly, it is submitted that the Examiner's reference to a "028/104 device, a '028/104/984 device" and the combined teachings of "the '028/104 reference or the '028/104/984 reference" is improper and without foundation because of *In re* Gordon, *supra*.

Accordingly, Applicants submit that claims 1, 6, 11, and 16 are allowable over Akram, Ho, and Chiu taken either singly or in combination.

Referring to claims 3, 8, 13, and 18, these dependent claims respectively depend from independent claims 1, 6, 11, and 16 and are believed to be allowable for the reasons set forth

above since they contain all the limitations set forth in the independent claims from which they depend and claim non-obvious combinations thereof.

Based on all of the above, it is respectfully submitted that claims 3, 8, 13, and 18 are allowable under 35 U.S.C. §103(a) as being patentable over Akram in view of Ho and further in view of Chiu.

This rejection should be reversed.

Rejection #3:

Summary of Akram:

Supra.

Summary of Ho:

Supra.

Summary of Chiu:

Supra.

Summary of Shin:

Shin is directed to a semiconductor package that has only one semiconductor chip. The heat sink [20] is exposed through the molding compound [50].

Arguments:

Claims 4, 9, 14, and 19 are improperly rejected under 35 U.S.C. 103(a) as being unpatentable over Akram in view of Ho further in view of Chiu and further in view of Shin.

Applicants respectfully traversed this rejection since the Applicants' claimed combination, as exemplified in claim 1, includes the limitation not disclosed in Akram, Ho, Chiu, or Shin of a semiconductor package having stacked dies in which:

> "the heat sink comprising a body portion, an undercut portion around a periphery thereof, and a plurality of legs integrally formed with the undercut portion"

With regard to claims 4, 9, 14, and 19, the Examiner has stated with respect to Shin:

> "The '511 patent, in disclosing a semiconductor package including a multilayered heat sink, teaches in the Abstract, Figs. 1 and 2, and column 1, lines 10-22, that an electrically conductive coating formed of silver or nickel and palladium as part of the heat sink results in an improvement in performance of the finally produced semiconductor package."

The Examiner concludes by stating:

> "Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the heat sink of the '028/104/984 reference such that the heat sink has an electrically conductive coating. One would have been motivated to make such a modification in view of the teachings by the '511 patent..."

Applicants respectfully traversed this rejection. As set forth above with respect to claims 1, 6, 11, and 16 it is respectfully submitted that the Examiner's proposed combination of Akram and Ho is improper because of *In re* Gordon, *supra* since each references teaches away from Applicants' invention, and even if combined result in an inoperable device.

Furthermore, as set forth above with respect to claims 3, 8, 13, and 18 Chiu is directed to a semiconductor package that has only one semiconductor chip. Accordingly, Chiu does not disclose or suggest a semiconductor package with stacked dies as claimed by Applicants.

Additionally, Shin is directed to a semiconductor package that has only one semiconductor chip. The heat sink [20] appears to be exposed through the molding compound [50]. An attempt to attach a second semiconductor chip to the exposed surface of the heat sink [20] would result in an inoperable device because the second semiconductor chip would be outside the semiconductor package. Applicants submit that a combination of references that results in an inoperable device is improper under 35 U.S.C. §103 because of *In re* Gordon, *supra*.

Since each of Akram, Ho, Chiu, and Shin teach away from Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103. Accordingly, it is submitted that the Examiner's reference to a "028/104 device, a '028/104/984 device" and the combined teachings of "the '028/104 reference or the '028/104/984 reference" is improper and without foundation because of *In re* Gordon, *supra*.

Accordingly, Applicants submit that claims 1, 6, 11, and 16 are allowable over Akram, Ho, Chiu, and Shin taken either singly or in combination.

Referring to claims 4, 9, 14, and 19, these dependent claims respectively depend from independent claims 1, 6, 11, and 16 and are believed to be allowable for the reasons set forth above since they contain all the limitations set forth in the independent claims from which they depend and claim non-obvious combinations thereof.

Based on all of the above, it is respectfully submitted that claims 4, 9, 14, and 19 are allowable under 35 U.S.C. 103(a) as being patentable over Akram in view of Ho further in view of Chiu and further in view of Shin.

This rejection should be reversed.

Rejection #4:

Summary of Ho:

Supra.

Summary of Akram:

Supra.

Arguments:

It is respectfully submitted that claims 1, 2, 5-7, 10-12, 15-17 and 20 are improperly rejected under 35 U.S.C. §103(a) as being unpatentable over Ho in view of Akram.

Applicants respectfully traversed this rejection since the Applicants' claimed combination, as exemplified in claim 1, includes the limitation not disclosed in Ho or Akram of a semiconductor package having stacked dies in which:

> "the heat sink comprising a body portion, an undercut portion around a periphery thereof, and a plurality of legs integrally formed with the undercut portion"

With regard to claims 1, 6, 11, and 16, the Examiner has stated:

> "Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the `104 patent' package such that the package comprises a second die so as to achieve increased density. A semiconductor package such modified hereinafter is referred to as the '104/028 device, and the combined teachings is referred to as the '104/028 reference, and a process for forming such a modified semiconductor package would

comprise attaching the second die to the heat sink and electrically connecting the second die to the substrate."

Applicants respectfully traversed this rejection.

Applicants agree with the Examiner that Ho:

"...fails to teach that the package comprises a second die, and thus fails to teach attaching a second die to the heat sink and electrically connecting the second die to the substrate."

Ho is directed to a semiconductor package in which only one semiconductor chip [31] is packaged with a heat sink [33] attached to the semiconductor chip [31] using solder balls [35]. Ho refers to FIG. 2 in pointing out the drawbacks of the structure of FIG. 2 (see column 2, lines 1-16). Applicants respectfully submit that Ho actually teaches away from the use of a heat sink in a semiconductor package as claimed by Applicants by listing what are perceived in Ho to be these drawbacks.

Furthermore, Ho does not disclose or suggest the use of the heat sink shown in FIG. 2 in a semiconductor package having stacked dies. Ho discloses the device in FIG. 2 as prior art. The structure shown in FIG. 2 of Ho shows a heat sink that is exposed through the molding compound of the semiconductor package rendering it impossible to attach an additional semiconductor chip to the heat sink in FIG. 2 because the second semiconductor chip would be outside the semiconductor package rendering the resulting device inoperable. Applicants submit that a combination of references that results in an inoperable device is improper under 35 U.S.C. §103 because of *In re* Gordon, *supra*.

In fact, U.S. Patent No. 5,997,626 to Wu, et al (hereinafter Wu), which is referred to by Ho with reference to FIG. 2 at column 1, lines 52-67 states that:

"Preferably the heat spreader [32] is exposed by the molding compound [30]." (see column 3, lines 53-55 of Wu)

Wu, the patent referred to by Ho, therefore does not disclose or suggest a semiconductor package for stacked dies as claimed by Applicants.

Ho does not disclose or suggest that more than one die may be stacked in a single package, and therefore teaches away from Applicants invention.

Akram is directed to the packaging of more than one integrated circuit devices within a common package. Akram discloses the use of a T-interposer between stacked dies in a

package. Applicants submit that Akram actually teaches away from Applicants invention as claimed.

Since both Ho and Akram teach away from Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103. Accordingly, it is submitted that the Examiner's reference to a "104/028 device, and the combined teachings of the '104/028 reference" is improper and without foundation because of *In re* Gordon, *supra*.

Accordingly, Applicants submit that claims 1, 6, 11, and 16 are allowable over Ho and Akram taken either singly or in combination because of *In re* Gordon, *supra*.

With regard to claims 2, 7, 12, and 17, the Examiner has stated:

> "Referring to claims 2, 7, 12, and 17, the '104/028 reference further discloses electrically connecting the first die (24) to the substrate uses a number of bonding wires (no number) and. attaching the modified heat sink attaches the modified heat sink that extends laterally over the number of bonding wires, that extends laterally over the lower die, and such that the undercut of the heat sink extends laterally over the number of bonding wires."

Referring to claims 2, 7, 12, and 17, these dependent claims respectively depend from independent claims 1, 6, 11, and 16 and are believed to be allowable for the reasons set forth above since they contain all the limitations set forth in the independent claims from which they depend and claim non-obvious combinations thereof.

With regard to claims 5, and 15, the Examiner has stated:

> "Referring to claims, 5 and 15, as evident from Figs. 5 and 9 of the `028 reference, the reference further discloses attaching a heat sink attaches a heat sink that extends laterally beyond the edges of the second die."

Applicants respectfully traversed this rejection. Referring to claims 5 and 15, these dependent claims respectively depend from independent claims 1 and 11 and are believed to be allowable for the reasons set forth above since they contain all the limitations set forth in the independent claims from which they depend and claim non-obvious combinations thereof.

With regard to claims 10 and 20, the Examiner has stated:

> "Referring to claims 10 and 20, as evident from Fig. 7 of the '028 reference, the reference further discloses providing a heat sink attaches a heat sink between each adjoining pair of dies in the stack of dies."

Applicants respectfully traversed this rejection. Referring to claims 10 and 20, these dependent claims respectively depend from independent claims 6 and 16 and are believed to be allowable for the reasons set forth above since they contain all the limitations set forth in the independent claims from which they depend and claim non-obvious combinations thereof.

This rejection should be reversed.

Rejection #5:

Summary of Ho:

Supra.

Summary of Akram:

Supra.

Summary of Chiu:

Supra.

Arguments:

It is respectfully submitted that claims 3, 8, 13, and 18 are improperly rejected under 35 U.S.C. §103(a) as being unpatentable over Ho in view of Akram and further in view of Chiu.

Applicants respectfully traversed this rejection since the Applicants' claimed combination, as exemplified in claim 1, includes the limitation not disclosed in Ho, Akram, or Chiu of a semiconductor package having stacked dies in which:

> "the heat sink comprising a body portion, an undercut portion around a periphery thereof, and a plurality of legs integrally formed with the undercut portion"

With regard to claims 3, 8, 13, and 18, the Examiner has stated:

> "Chiu, in disclosing a thermally enhanced chip scale package having a heat sink (114, Fig. 1B), teaches that the heat sink may be wire bonded to a ground connection to provide the packaged integrated circuit with shielding from electrical or electromagnetic interference (column 2, lines 16-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '104/028 reference's heat sink so that the heat sink is electrically grounded using wire bonding. One would have been motivated to make such a modification in view of the teachings by Chiu that

ground connection using wire bonding provide the packaged integrated circuit with shielding from electrical or electromagnetic interference. A semiconductor package such modified hereinafter is referred to as the '104/028/984 device, and the combined teachings is referred to as the 104/028/984 reference."

Applicants respectfully traversed this rejection. As set forth above with respect to claims 1, 6, 11, and 16 it is respectfully submitted that the Examiner's proposed combination of Ho and Akram is improper because of *In re* Gordon, *supra* since each references teaches away from Applicants' invention, and if combined result in an inoperable device.

Furthermore, Chiu is directed to a semiconductor package that has only one semiconductor chip. Accordingly, Chiu does not disclose or suggest a semiconductor package with stacked dies as claimed by Applicants.

Since each of Ho, Akram, and Chiu teach away from Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103. Accordingly, it is submitted that the Examiner's reference to a "'104/028 device, a '104/028/984 device" and the combined teachings of "the '104/028 reference or the '104/028/984 reference" is improper and without foundation because of *In re* Gordon, *supra*.

Accordingly, Applicants submit that claims 1, 6, 11, and 16 are allowable over Ho, Akram, and Chiu taken either singly or in combination because of *In re* Gordon, *supra*.

Referring to claims 3, 8, 13, and 18, these dependent claims respectively depend from independent claims 1, 6, 11, and 16 and are believed to be allowable for the reasons set forth above since they contain all the limitations set forth in the independent claims from which they depend and claim non-obvious combinations thereof.

Based on the above, it is respectfully submitted that claims 3, 8, 13, and 18 are allowable under 35 U.S.C. 103(a) as being patentable over Ho in view of Akram and further in view of Chiu.

This rejection should be reversed.

Serial No.: 10/825,910
Group Art Unit: 2818

Rejection #6

Summary of Ho:

Supra.

Summary of Akram:

Supra.

Summary of Chiu:

Supra.

Summary of Shin:

Supra.

Arguments:

It is respectfully submitted that claims 4, 9, 14, and 19 are improperly rejected under 35 U.S.C. §103(a) as being unpatentable over Ho in view of Akram in further view of Chiu and further in view of Shin.

Applicants respectfully traversed this rejection since the Applicants' claimed combination, as exemplified in claim 1, includes the limitation not disclosed in Ho, Akram, Chiu, or Shin of a semiconductor package having stacked dies in which:

> "the heat sink comprising a body portion, an undercut portion around a periphery thereof, and a plurality of legs integrally formed with the undercut portion"

With regard to claims 4, 9, 14, and 19, the Examiner has stated with respect to Shin:

> "The '511 patent, in disclosing a semiconductor package including a multilayered heat sink, teaches in the Abstract, Figs. 1 and 2, and column 1, lines 10-22, that an electrically conductive coating formed of silver or nickel and palladium as part of the heat sink results in an improvement in performance of the finally produced semiconductor package."

The Examiner concludes by stating:

> "Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the heat sink of the '104/028/984 reference such that the heat sink has an electrically conductive coating. One would have been motivated to make such a modification in view

> of the teachings by the '511 patent that an electrically conductive coating formed of silver or nickel and palladium as part of the heat sink results in an improvement in performance of the finally produced semiconductor package."

Applicants respectfully traversed this rejection. As set forth above with respect to claims 1, 6, 11, and 16 it is respectfully submitted that the Examiner's proposed combination of Ho and Akram is improper because of *In re* Gordon, *supra* since each references teaches away from Applicants' invention, and if combined result in an inoperable device.

Furthermore, as set forth above with respect to claims 3, 8, 13, and 18 Chiu is directed to a semiconductor package that has only one semiconductor chip. Accordingly, Chiu does not disclose or suggest a semiconductor package with stacked dies as claimed by Applicants.

Additionally, Shin is directed to a semiconductor package that has only one semiconductor chip. The heat sink [20] appears to be exposed through the molding compound [50]. An attempt to attach a second semiconductor chip to the exposed surface of the heat sink [20] would result in an inoperable device because the second semiconductor chip would be outside the semiconductor package. Applicants submit that a combination of references that results in an inoperable device is improper under 35 U.S.C. §103 because of *In re* Gordon, *supra.*

Since each of Ho, Akram, Chiu, and Shin teach away from Applicants' invention, it is respectfully submitted that there is no teaching or suggestion to combine the references to arrive at Applicants' invention as required by 35 USC §103. Accordingly, it is submitted that the Examiner's reference to a "'104/028 device, a '104/028/984 device" and the combined teachings of "the '104/028 reference or the '104/028/984 reference" is improper and without foundation because of *In re* Gordon, *supra.*

Accordingly, Applicants submit that claims 1, 6, 11, and 16 are allowable over Akram, Ho, Chiu, and Shin taken either singly or in combination because of *In re* Gordon, *supra.*

Referring to claims 4, 9, 14, and 19, these dependent claims respectively depend from independent claims 1, 6, 11, and 16 and are believed to be allowable for the reasons set forth above since they contain all the limitations set forth in the independent claims from which they depend and claim non-obvious combinations thereof.

Based on the above, it is respectfully submitted that claims 4, 9, 14, and 19 are allowable under 35 U.S.C. 103(a) as being patentable over Ho in view of Akram further in view of Chiu and further in view of Shin.

This rejection should be reversed.

(10) ***Conclusion and Relief Requested:***

With respect to the issues presented in this appeal as set forth above in section (6), Applicants hereby solicit a ruling that:

(a) The restriction requirement issued after final rejection in response to Applicants' Pre-Appeal Brief Request for Review was improper and should be withdrawn.

(b) Claims 1, 2, 5-7, 10-12, 15-17, and 20 were improperly rejected under 35 U.S.C. §103(a) as being unpatentable over Akram in view of Ho. This rejection should be reversed.

(c) Claims 3, 8, 13, and 18 were improperly rejected under 35 U.S.C. §103(a) as being unpatentable over Akram in view of Ho and further in view of Chiu. This rejection should be reversed.

(d) Claims 4, 9, 14, and 19 were improperly rejected under 35 U.S.C. §103(a) as being unpatentable over Akram in view of Ho further in view of Chiu and further in view of Shin. This rejection should be reversed.

(e) Claims 1, 2, 5-7, 10-12, 15-17 and 20 were improperly rejected under 35 U.S.C. §103(a) as being unpatentable over Ho in view of Akram. This rejection should be reversed.

(f) Claims 3, 8, 13, and 18 were improperly rejected under 35 U.S.C. §103(a) as being unpatentable over Ho in view of Akram and further in view of Chiu. This rejection should be reversed.

Serial No.: 10/825,910
Group Art Unit: 2818

(g) Claims 4, 9, 14, and 19 were improperly rejected under 35 U.S.C. §103(a) as being unpatentable over Ho in view of Akram further in view of Chiu and further in view of Shin. This rejection should be reversed.

Claims 1-20 are patentable over the prior art, and a Notice of Allowance to that effect should be issued.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including any extension of time fees, to Deposit Account No. 50-0374 and please credit any excess fees to such deposit account.

Respectfully submitted,

Mikio Ishimaru

Mikio Ishimaru
Registration No. 27,449

The Law Offices of Mikio Ishimaru
333 W. El Camino Real, Ste. 330
Sunnyvale, CA 94087
Telephone: (408) 738-0592
Fax: (408) 738-0881
Date: November 30, 2005

Appendix I – Claims on Appeal (on following page)

Serial No.: 10/825,910
Group Art Unit: 2818

CLAIMS ON APPEAL

1. A method of assembling a semiconductor package with stacked dies comprising:

providing a substrate;

attaching a first die to the substrate;

electrically connecting the first die to the substrate;

attaching a heat sink to the first die;

the heat sink comprising a body portion, an undercut portion around a periphery thereof, and a plurality of legs integrally formed with the undercut portion;

attaching the plurality of legs to the substrate;

attaching a second die to the heat sink;

electrically connecting the second die to the substrate; and

encapsulating the first die, the heat sink, and the second die.

2. The method of assembling a semiconductor package with stacked dies as claimed in claim 1 wherein:

electrically connecting the first die to the substrate uses a number of bonding wires; and

attaching a heat sink attaches a heat sink that extends laterally over the number of bonding wires.

3. The method of assembling a semiconductor package with stacked dies as claimed in claim 1 wherein attaching a heat sink attaches a heat sink that is electrically grounded.

4. The method of assembling a semiconductor package with stacked dies as claimed in claim 1 wherein attaching a heat sink attaches a heat sink that has an electrically conductive coating, further comprising:

connecting the second die to the electrically conductive coating; and

connecting the electrically conductive coating to a ground plane.

5. The method of assembling a semiconductor package with stacked dies as claimed in claim 1 wherein attaching a heat sink attaches a heat sink that extends laterally beyond the edges of the second die.

6. A method of thermally enhancing a semiconductor package with a stack of dies comprising providing a heat sink between dies in the stack; the heat sink having a body portion, an undercut portion around a periphery thereof, and a plurality of legs integrally formed with the undercut portion.

7. The method of thermally enhancing a semiconductor package with a stack of dies as claimed in claim 6 wherein:

providing a heat sink attaches a heat sink that extends laterally over the lower die to which the heat sink is attached.

8. The method of thermally enhancing a semiconductor package with a stack of dies as claimed in claim 6 wherein providing a heat sink attaches a heat sink that is electrically grounded.

9. The method of thermally enhancing a semiconductor package with a stack of dies as claimed in claim 6 wherein providing a heat sink attaches a heat sink that has an electrically conductive coating, further comprising:

connecting one of the dies in the stack of dies to the electrically conductive coating; and

connecting the electrically conductive coating to a ground plane.

10. The method of thermally enhancing a semiconductor package with a stack of dies as claimed in claim 6 wherein providing a heat sink attaches a heat sink between each adjoining pair of dies in the stack of dies.

11. A semiconductor package with stacked dies comprising:

a substrate;

a first die attached to the substrate;

the first die being electrically connected to the substrate;

a heat sink attached to the first die;

the heat sink having a body portion, an undercut portion around a periphery thereof, and a plurality of legs integrally formed with the undercut portion;

the plurality of legs attached to the substrate;

a second die attached to the heat sink and electrically connected to the substrate; and

an encapsulant over the first die, the heat sink, and the second die.

12. The semiconductor package with stacked dies as claimed in claim 11 further comprising:

a number of bonding wires electrically connecting the first die to the substrate; and

wherein:

the undercut of the heat sink extends laterally over the number of bonding wires.

13. The semiconductor package with stacked dies as claimed in claim 11 wherein the heat sink is electrically grounded.

14. The semiconductor package with stacked dies as claimed in claim 11 wherein:

the heat sink has an electrically conductive coating connected to a ground plane on the substrate; and

the second die is connected to the electrically conductive coating.

15. The semiconductor package with stacked dies as claimed in claim 11 wherein the undercut of the heat sink extends laterally beyond the edges of the second die.

16. A thermally enhanced semiconductor package with a stack of dies comprising:

a heat sink between dies in the stack;

the heat sink having a body portion, an undercut portion around a periphery thereof, and a plurality of legs integrally formed with the undercut portion.

17. The thermally enhanced semiconductor package with a stack of dies as claimed in claim 16 wherein:

the undercut of the heat sink extends laterally over the die to which the heat sink is attached.

18. The thermally enhanced semiconductor package with a stack of dies as claimed in claim 16 wherein the heat sink is electrically grounded.

19. The thermally enhanced semiconductor package with a stack of dies as claimed in claim 16 wherein:

the heat sink has an electrically conductive coating;

one of the dies in the stack of dies is connected to the electrically conductive coating; and

the electrically conductive coating is connected to a ground plane.

20. The thermally enhanced semiconductor package with a stack of dies as claimed in claim 16 wherein a heat sink is positioned between each adjoining pair of dies in the stack of dies.